(Larger fans-in → more capacitances → reduced performance)

Four inputs AND

Four input AND

Involved, for example: \[ F = ABCD + AB\overline{D} + \overline{A}B + \overline{A}C \]

Fan-ins due to the partially late # of literals

Now with four inputs, we need four gates with late gate.

However, they may require fewer gates with a good # of literals.

The best networks are fast (two-gate levels) and or-and (I0-0), NAND-NAND (from pos), NOR-NOR (from pos).

Provide minimum two-level logic networks: AND-OR (5-0), NOR-NOR (4-3).

Methods such as K-maps, Quine-McCluskey, exeedeso, etc.

Multi-level simplification

Lecture 18
Only AND Gates

Only NOR Gates

Only 2-Input Gates are available

Technologies - Preparation Stage

Substitution, AND Carvering, etc.

Factoring, Decomposition, Extraction.

Techniques:

Gate Level (More Delays)
Reduced Fan-in By 2"/Input & Pruning: Improving The

Technological - Implementation Stage

Synthesis Process
2-input Gates
3 levels
5 literals

S-input Gates
2 levels
9 literals

\[ F = (A+B)(C+D) + E \]

\[ F = AC + AD + BD + CE + E \]

Factorization Techniques
4 Levels
2.4 Input Gates
3.2 Output Gates

\[ F = A B + (A + B) (C + D) \]

\[ F = A B (C + D) + A B (C + D) \]

\[ F = A B (C + D) + (A + B) (C + D) \]

\[ F = A B (C + D) + (A + B) (C + D) \]

\[ F = A B + A B (C + D) + A B (C + D) \]

\[ F = A B (C + D) + (A + B) (C + D) \]
\[ y = \overline{B} \]
\[ x = (A + B) \]
\[ y = \overline{E} \]
\[ M = \overline{CDE} \]
\[ N = (A + B) \overline{E} \]
\[ C = (A + B) \overline{E} \]
\[ F = (A + B) \overline{CDE} + \overline{E} \]
\[ E = xy + \overline{E} \]

("Deconversion" of a collection of functions)
\[ \begin{align*}
& F = A + BCD \\
& = A + ACD + BCD \\
& = A + AD + A3C + 3CD \\
& = A + AD + A3C + BCD \\
& = (A + BC)(A + D) \\
& \text{Substitution} \quad F = C(A + D) \\
& \text{Substitution} \quad F = A + BCD \\
& \text{Collecting} \quad F = A + BCD
\end{align*} \]
Example: \( E = A(\overline{B} + \overline{C}) + \overline{E} \)

NOR/NOR Gates

(2 NOR Gates)

\[ \frac{\text{NOR/NAND Gates}}{\text{NAND/NAND Gates}} \]