Lecture 30

Notes:

- All have been returned

- Lab: Present
- Send email to Kasuma (mostly assembly language)

- Chapters
- Katz: 1 to 4 & App. A
- Miller: 1 to 5

Test: This Friday, Apr 18th
(3) At least one feedback path from the output to the input.

(2) Inputs must follow a specific sequence.

(1) Outputs appear on one or more inputs in time.

Sequential logic.

(2) No feedback path from output to the input.

(1) Outputs only depend on a combination of the inputs at the present stage of the inputs.

Combinational logic.
SET - RESET (RS)

Flip-Flop

Binary Cell, which locks either A or B.

Each Binary input (BIT) is stored in a

To replace its value, Binary Values can be changed until completed.

Memory: Some remain in which the
As \( E^{n+1} \) (for \( t = n+1 \) )

As \( E^n \) (for \( t = n \)) and \( \text{not output} \)

We will refer to the input \( \emptyset \& \emptyset \) and both outputs \( \text{not inputs} \). For the

Circuit

\( \text{reset} & \text{ resets a} \quad 0 \)

\( \text{set} & \text{ resets a} \quad 1 \)

\text{standard form:} \quad \text{same circuit can be as drawn in text} \)
Given the input states 0 B A, the next state is 1. The characteristic table shows the states and their transitions:

**Characteristic Table**

<table>
<thead>
<tr>
<th>Input</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Set</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Reset</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Left A</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
State Diagram of a RS Flip-Flop
A special but *un*terminating state

In practice, one or the outputs (0 or 0) will

In theory, the output would oscillate (see below)

Output becomes unstable (unterminating)

<table>
<thead>
<tr>
<th>! ! ! ! ! ! ! !</th>
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</table>

Because:

\[ R = S = 1 \]

\[ \text{Characteristics Table} \]
To avoid similar situations, see circuits and

A Vin 1 Time When They Are Valid

Clocked so that the inputs are sampled only