(Ripple)

\[ \begin{array}{c|ccc}
\text{Out} & 1 & 0 & 0 \\
\hline
\text{In} & 1 & 1 & 0 \\
\end{array} \]

\[ f_{n+1} = f_n \]

Flip-Flop

Flop-Flop
2) Use "Master-Slave" Construction

Solutions:
1) Make CLK pulse shorted from the propagation delay.

Output will toggle when \( \overline{Q} \neq \overline{K} = 1 \). The output looks as \( Q' \) is

![Diagram](image_url)
An initial state.

Some times, if's also present @i.e., current asynchronous inputs.

F & K are "synchronous" inputs.

(Receiving edge)
(Leading edge)
(Paused edge)
(Falling edge)
(Receiving edge)
(Leading edge)
(Paused edge)
(Falling edge)

Flip-Flops
General Model for Clocked Flip-Flops

Recall:

D-FF

JK-FF
The basic cell

The correct input signals go

Preceding in order to generate

We need to begin the Set-Reset.

For a given characteristic table,

Reesign:

inputs

CLK

Q

Q

@ (ASYNCH)

Reset

Set

Reset/Reset

Set/Reset

(qwe, etc.)

Set/Reset
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<th>Characteristic</th>
<th>Table of A 2-RS-FF</th>
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<tr>
<td></td>
<td>$C_{K}$  (D_{n+1})  3  $R$</td>
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<tr>
<td>Basic Cell</td>
<td>Input (Input)</td>
</tr>
<tr>
<td></td>
<td>$A$ (R-S) 3-state Cell</td>
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<tr>
<td></td>
<td>$2$-Type FF Logic</td>
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</table>
ECDC04

Clock Circuit

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Flip-flop "B"

Inputs

Clock

Comb. logic

Counters

From FF A to B
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</tbody>
</table>

### Notes:

- **A**ssume **3**-**R** in **F** already **C**ompleted  
- **C**onvert to **2**-**F**

---

**Steps**:

1. Verify that the **3**-**R** is compatible with the **2**-**F**.
2. Make necessary adjustments to the **3**-**R** to align with the **2**-**F**.

---

**Initialization**:

- If the **3**-**R** is already complete, proceed to the next step.
- Convert the **3**-**R** to a **2**-**F** to ensure compatibility.