### Table

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AX</td>
<td>123</td>
</tr>
<tr>
<td>BX</td>
<td>456</td>
</tr>
<tr>
<td>CX</td>
<td>789</td>
</tr>
<tr>
<td>DX</td>
<td>012</td>
</tr>
<tr>
<td>SI</td>
<td>321</td>
</tr>
<tr>
<td>DI</td>
<td>654</td>
</tr>
<tr>
<td>BP</td>
<td>987</td>
</tr>
<tr>
<td>SP</td>
<td>210</td>
</tr>
<tr>
<td>IP</td>
<td>765</td>
</tr>
</tbody>
</table>

### Diagram

- Stack Pointer
- EIP
- EBP
- ESP
- ESI
- EDI
- ESI
- ESI
- ESI
- ESI

### Notes
- Program mode
- The execute
- Use 4
AC (AVliment Cat. Check - 48) (46)

(386-up)

(386-up)

(266-up)

(266-up)

(86-up)

OS/2

- Cary, Parity, AX Carry, EAX.

- Cx Carry, Parity, AX Carry, EAX.

- Fl/Ass.

- 64/16/32/64/8.

- 386-Cone 2

- 88/86/286

- 8/86/286

- Special

- 88/86/286

- 386/686m

- Rip, Eip, Eip
Offset = 0
Segment address = 0

Segment = 42A0

Offset = 0

Physical
Address

Offset

SEGFNT

Virtual

Memory

Section of

Segment = 491C bytes

Real Mode Memory Addresses
Learning Programs (recognition)

Default: $\text{seg: CS} \Rightarrow \text{ESP}$

$\text{gs: no segment}$
$\text{fs: no segment}$

S: $\text{ES} \Rightarrow \text{EAX/CES/EFS/ECX/ECI/EFI}$

S: $\text{ESP/ESP}$

$\text{CS: ESP}$

Note: How many different ways of addressing the same EA are there?

\[
\begin{align*}
\phi & \phi A, A \\
\phi & \phi A, 0 \\
\phi & 0, 0 \\
\phi & 0, 0 \\
\phi & 0, 0 \\
\phi & 0, 0 < 4,200:0,400 \\
4,200:0,400 & = 0,400 \\
0,400 & = 0,400
\end{align*}
\]

The same effective address could be achieved w/ (for ex.)
L-Qaeda

Detected Access
Access Rights
- Description: Byte + Limit
- System (Global) ≠ Application (Local)
- 8192 Possible descriptors in each of two modes:
  - 32-bit ≠ 64-bit preferred modes (PIE or NP)
  - Offset can be (386-up) or 32-bit registers

A segment register acts as a selector for Memory Addresses

Protected Memory Addresses
First Memory Address is 0 - No Protection

Address

\[ \text{Table} + \text{offset} = \text{Physical} \]

\[ \text{Page table} + \text{Page} = \text{Page dir.} \]

Physical Address = CR3 + dir = Page dir.

\[
\begin{array}{|c|c|c|}
\hline
12-bits & 10-bits & 10-bits \\
\hline
\end{array}
\]

Page Size: 4K, Page Table, Offset

- Control Registers: CR0 - CR4

- Processor Cache

- Index Register: CTIR / CDIR

Invisible Registers: -